

FEATURES

Low offset voltage: 100 μ V maximum
Low input bias current: 1 pA maximum
Single-supply operation: 5 V to 16 V
Low noise: 10 nV/ $\sqrt{\text{Hz}}$
Wide bandwidth: 4 MHz
Unity-gain stable
Small package options
 3 mm \times 3 mm LFCSP_VD
 8-lead SOIC_N
 8-lead MSOP

APPLICATIONS

Sensors
Medical equipment
Consumer audio
Photodiode amplification
ADC drivers

GENERAL DESCRIPTION

The AD8661/AD8662 are rail-to-rail output, single-supply amplifiers that use the Analog Devices patented DigiTrim[®] trimming technique to achieve low offset voltage. The AD8661/AD8662 feature extended operating ranges with supply voltages up to 16 V. They also feature low input bias current, wide signal bandwidth, and low input voltage and current noise.

The combination of low offset, very low input bias current, and a wide supply range make these amplifiers useful in a wide variety of applications usually associated with higher priced JFET amplifiers. Systems using high impedance sensors, such as photodiodes, benefit from the combination of low input bias

current, low noise, low offset, and wide bandwidth. The wide operating voltage range meets the demands of high performance ADCs and DACs. Audio applications and medical monitoring equipment can take advantage of the high input impedance, low voltage and current noise, and wide bandwidth.

The single AD8661 is available in an 8-lead SOIC_N package and an 8-lead LFCSP_VD. The AD8661 SOIC_N package is specified over the extended industrial temperature range from -40°C to $+125^{\circ}\text{C}$. The AD8661 LFCSP_VD is specified over the extended industrial temperature range from -40°C to $+85^{\circ}\text{C}$. The AD8662 is available in an 8-lead SOIC_N package and an 8-lead MSOP specified over the extended industrial temperature range from -40°C to $+125^{\circ}\text{C}$.

PIN CONFIGURATIONS

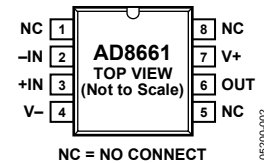


Figure 1. AD8661, 8-Lead SOIC_N (R-8)

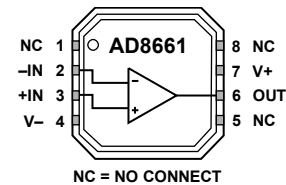


Figure 2. AD8661, 8-Lead LFCSP_VD (CP-8-2)

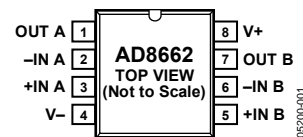


Figure 3. AD8662, 8-Lead SOIC_N (R-8)

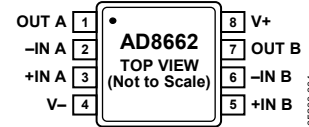


Figure 4. AD8662, MSOP (RM-8)

Rev. C

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REVISION HISTORY

5/06—Rev. B to Rev. C

Changes to Ordering Guide	13
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3/06—Rev. A to Rev. B

Added AD8662	Universal
Added MSOP	Universal
Changes to Table 1.....	3
Changes to Table 2.....	4
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Updated Outline Dimensions	13
Changes to Ordering Guide	13

1/06—Rev. 0 to Rev. A

Added LFCSP_VD	Universal
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Ordering Guide	13

9/05—Revision 0: Initial Version

SPECIFICATIONS

AD8661/AD8662 ELECTRICAL CHARACTERISTICS

$V_S = 5.0\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1. AD8661/AD8662 SOIC_N and MSOP Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_S = 8\text{ V}$, $V_{CM} = 3\text{ V}$ $V_{CM} = -0.1\text{ V to }+3.0\text{ V}$			100	μV
AD8661		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		30	200	μV
AD8661		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1200	μV
AD8662		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1400	μV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.5	pA
Input Voltage Range			-0.1		+3.0	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.1\text{ V to }+3.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	85	100		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$	80	100		dB
Offset Voltage Drift			100	240		V/mV
AD8661	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	10	$\mu\text{V}/^\circ\text{C}$
AD8662	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	9	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.85	4.93		V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.80	50	100	mV
Short-Circuit Current	I_{SC}			± 19	120	mV
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		65		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to }16\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	110		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	115		dB
				1.15	1.40	mA
					2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		3.5		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_o			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
	e_n	$f = 10\text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

AD8661/AD8662

$V_S = 16\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2. AD8661/AD8662 SOIC_N and MSOP Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_S = 8\text{ V}$, $V_{CM} = 3\text{ V}$ $V_{CM} = -0.1\text{ V to }+14.0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			100 35 200 1200 1400 1000	μV μV μV μV μV μV
AD8661						
AD8661						
AD8662						
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	1 50 300	pA pA pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.5 20 75	pA pA pA
Input Voltage Range			-0.1		+14	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.1\text{ V to }+14.0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	90	110		dB dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }15.5\text{ V}$	200	420		V/mV
Offset Voltage Drift						$\mu\text{V}/^\circ\text{C}$
AD8661	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	10	
AD8662	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	9	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	15.93 15.60 15.50	15.97 15.70		V V V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		24 210	50 350 450	mV mV mV
Short-Circuit Current	I_{SC}			± 140		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		45		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to }16\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	95 95	110 115		dB dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.25	1.55 2.1	mA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		3.5		V/ μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_o			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		12		nV/ $\sqrt{\text{Hz}}$
	e_n	$f = 10\text{ kHz}$		10		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$

AD8661 ELECTRICAL CHARACTERISTICS—LFCSP_VD ONLY

$V_S = 5.0\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3. AD8661 LFCSP_VD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_S = 8\text{ V}$, $V_{CM} = 3\text{ V}$ $V_{CM} = -0.1\text{ V to }+3.0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$			150	μV
				50	300	μV
					2000	μV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.3	1	pA
					50	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2	0.5	pA
					20	pA
Input Voltage Range Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.1\text{ V to }+3.0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	-0.1		+3.0	V
			85	100		dB
Large Signal Voltage Gain Offset Voltage Drift	A_{VO} $\Delta V_{OS}/\Delta T$	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80	100		dB
			100	240		V/mV
			4		17	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	4.85	4.93		V
			4.80			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		50	100	mV
					120	mV
Short-Circuit Current	I_{SC}			± 19		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		65		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to }16\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	95	110		dB
			95	115		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		1.15	1.40	mA
					1.8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		3.5		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$\angle\phi_o$			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

AD8661/AD8662

$V_S = 16\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4. AD8661 LFCSP_VD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_S = 8\text{ V}$, $V_{CM} = 3\text{ V}$ $V_{CM} = -0.1\text{ V to } +14.0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		50	150	μV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.3	1	μA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2	0.5	μA
Input Voltage Range			-0.1		+14	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.1\text{ V to } +14.0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	90	110		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to } 15.5\text{ V}$	200	420		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		4	17	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	15.95 15.60 15.50	15.97 15.70		V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		24 210	50 350	mV
Short-Circuit Current	I_{SC}			± 140	400	mV
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		45		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to } 16\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	95	110		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	95	115	1.25 1.55 1.9	dB mA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		3.5		V/ μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_o			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		12		nV/ $\sqrt{\text{Hz}}$
	e_n	$f = 10\text{ kHz}$		10		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	GND to V_S
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-60°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N	121	43	°C/W
8-Lead LFCSP_VD	75 ¹	18 ¹	°C/W
8-Lead MSOP	142	44	°C/W

¹ Exposed pad soldered to application board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

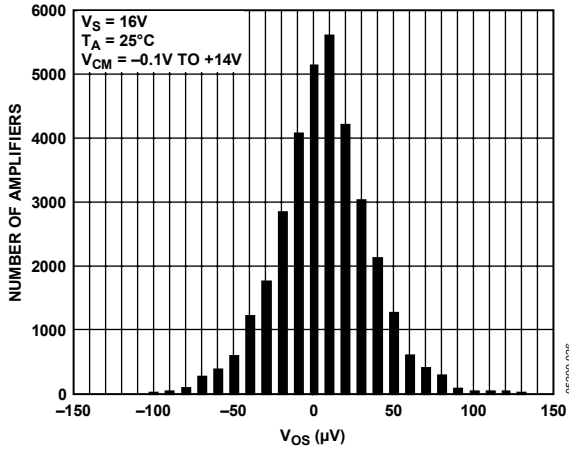


Figure 5. Input Offset Voltage Distribution

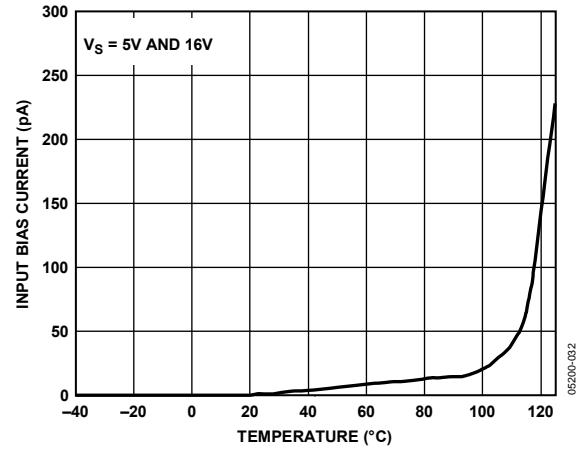


Figure 8. Input Bias Current vs. Temperature

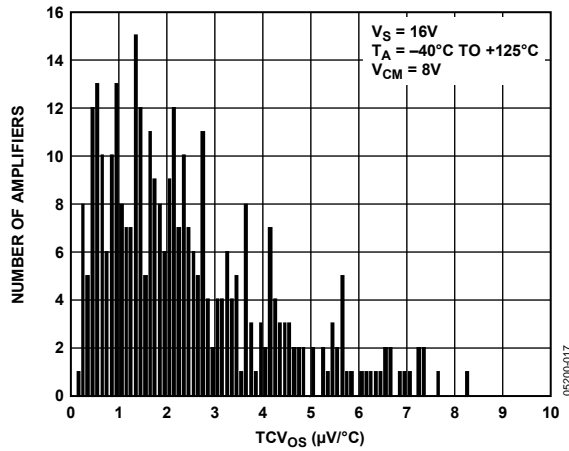


Figure 6. Offset Voltage Drift Distribution

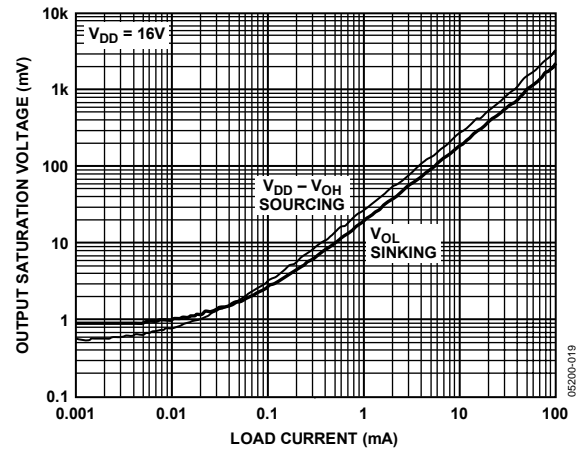


Figure 9. Output Swing vs. Load Current

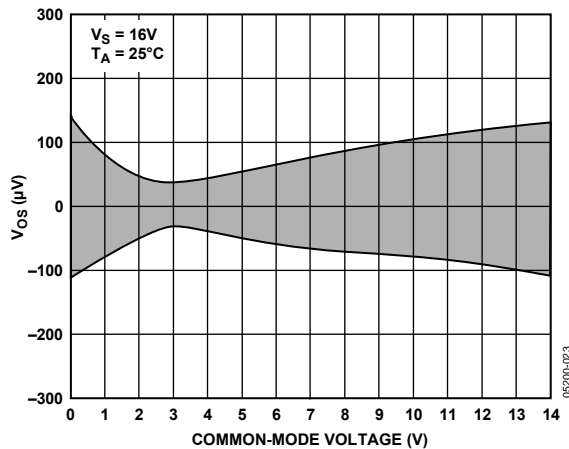


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

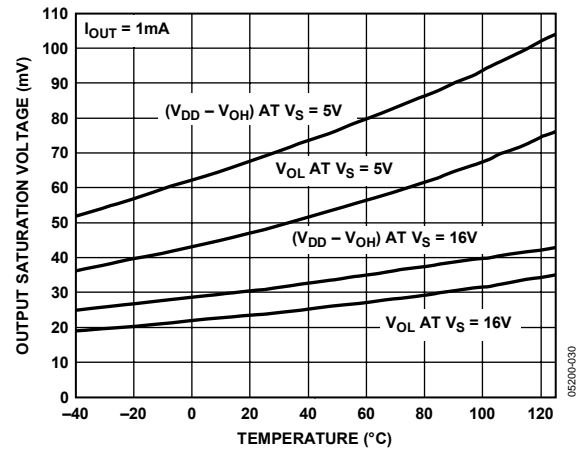


Figure 10. Output Swing vs. Temperature, $I_{OUT} = 1\text{ mA}$

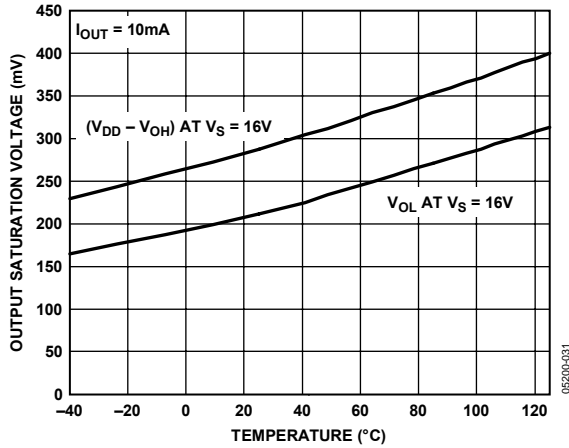


Figure 11. Output Swing vs. Temperature, $I_{OUT} = 10\text{ mA}$

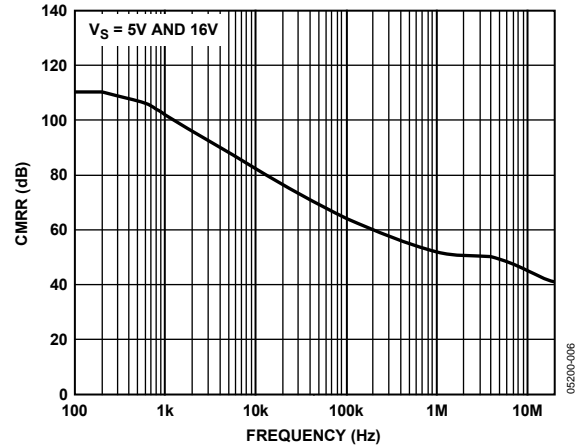


Figure 14. CMRR vs. Frequency

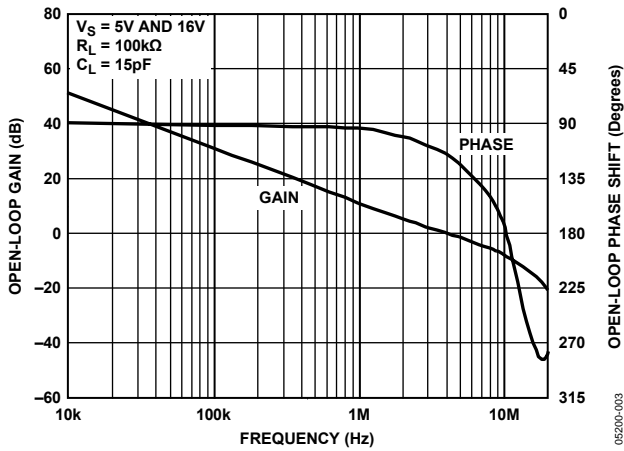


Figure 12. Open-Loop Gain and Phase vs. Frequency

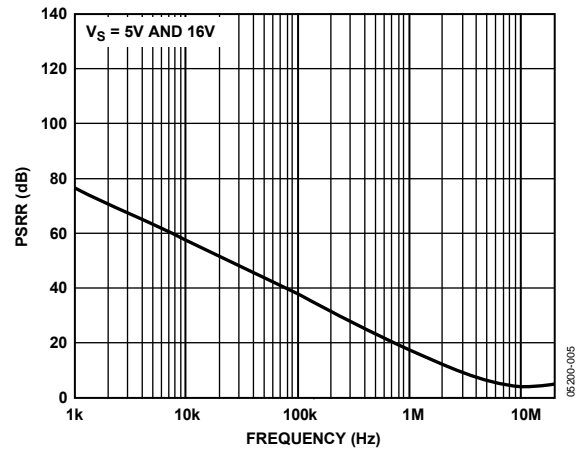


Figure 15. PSSR vs. Frequency

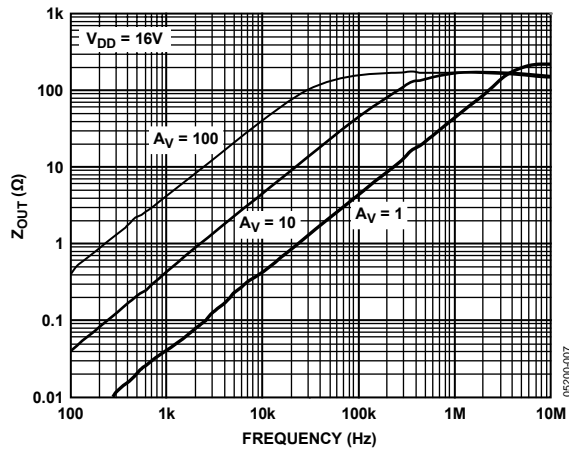


Figure 13. Closed-Loop Output Impedance vs. Frequency

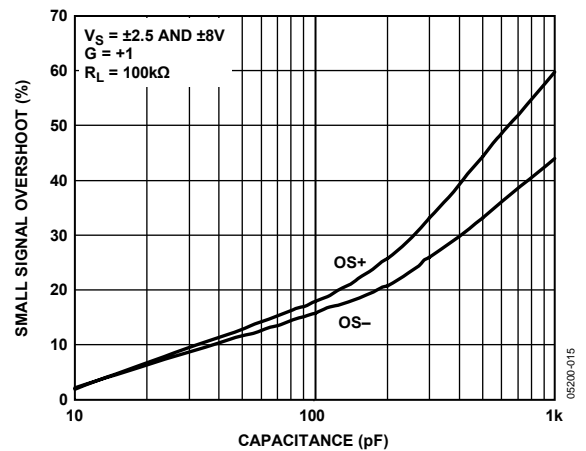


Figure 16. Small Signal Overshoot vs. Load Capacitance

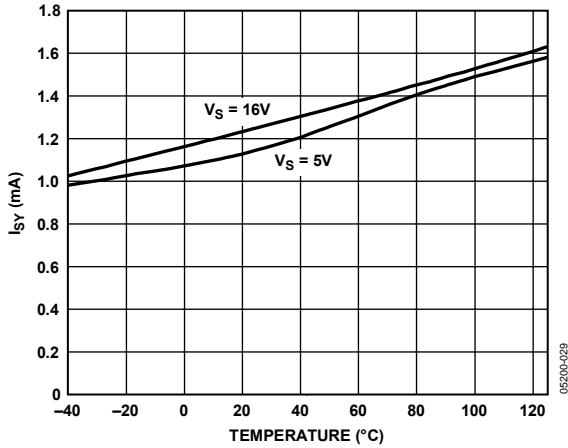


Figure 17. Supply Current (I_{SV}) vs. Temperature

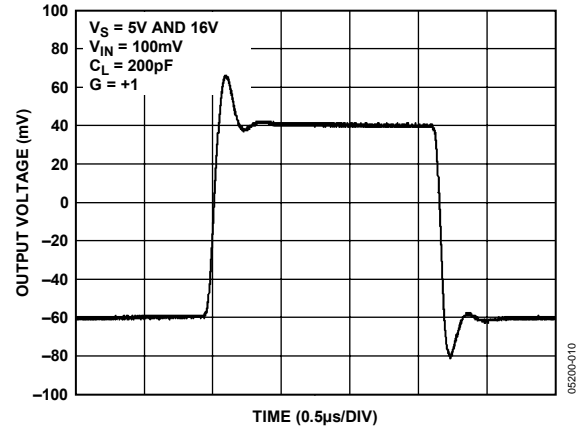


Figure 20. Small Signal Transient Response

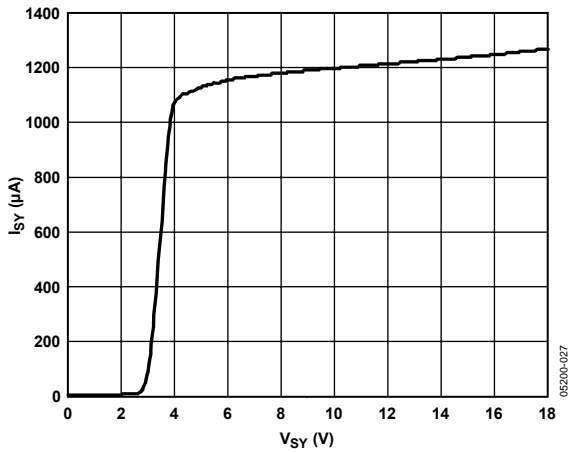


Figure 18. Supply Current (I_{SV}) vs. V_{SV} (Dual-Supply Configuration, $T_A = 25^\circ\text{C}$)

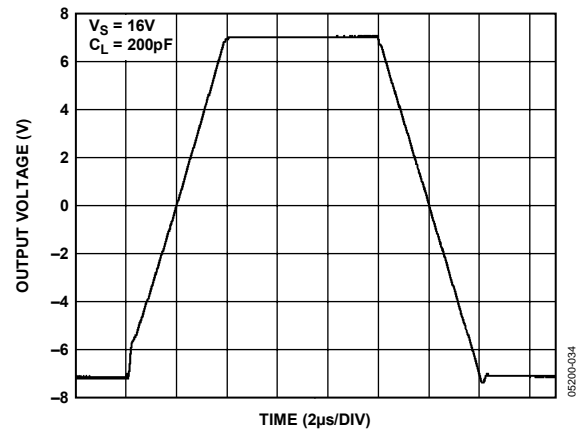


Figure 21. Large Signal Transient Response

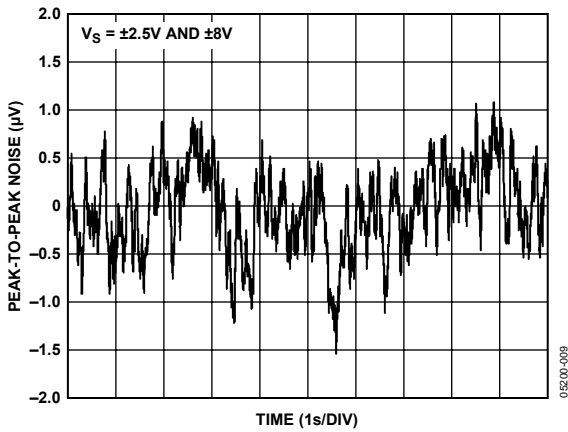


Figure 19. 0.1 Hz to 10 Hz Input Voltage Noise

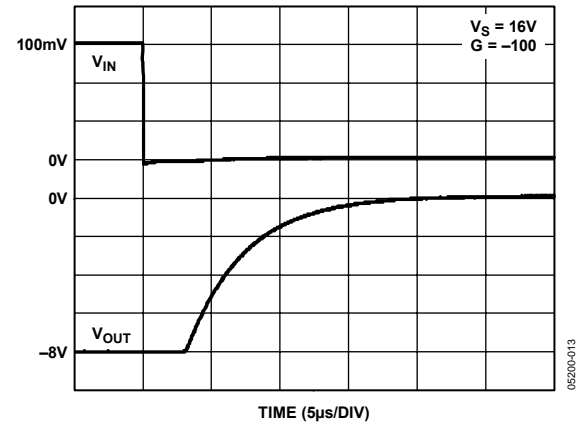


Figure 22. Positive Overload Recovery

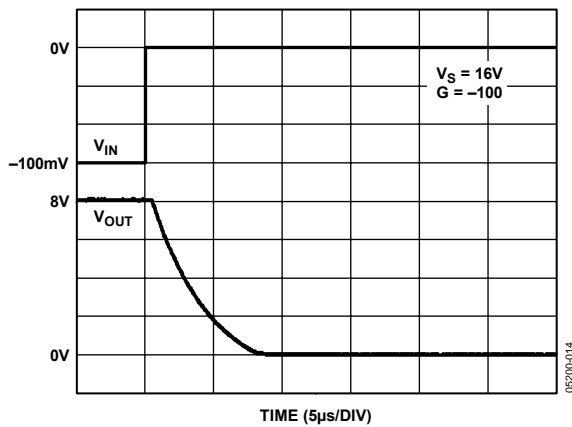


Figure 23. Negative Overload Recovery

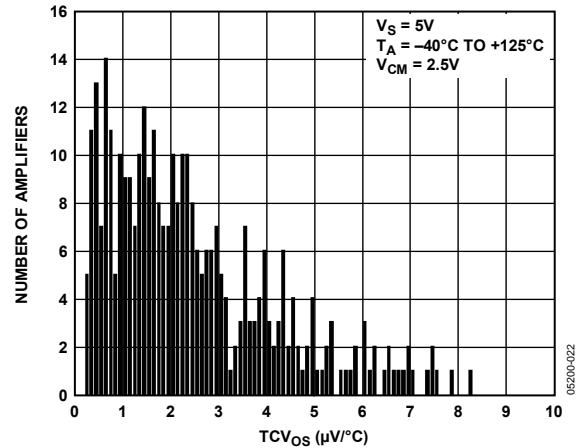


Figure 26. Offset Voltage Drift Distribution

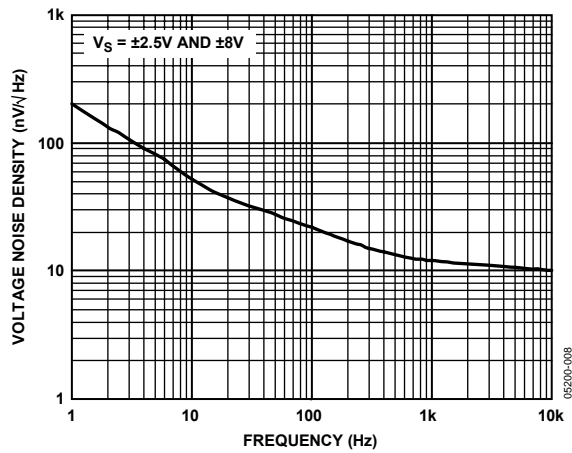


Figure 24. Voltage Noise Density vs. Frequency

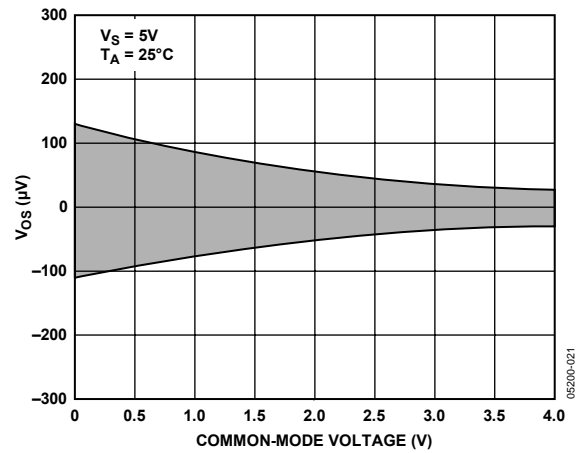


Figure 27. Input Offset Voltage vs. Common-Mode Voltage

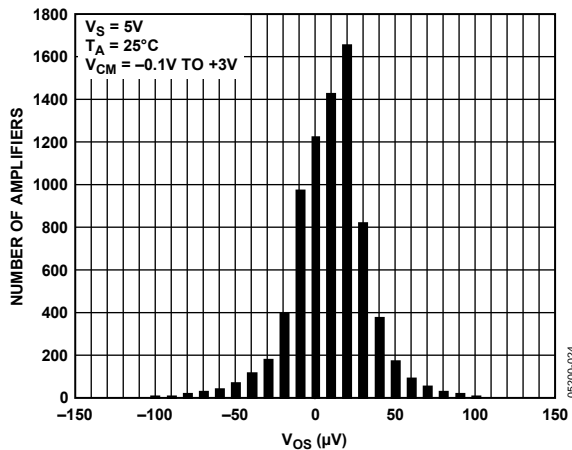


Figure 25. Input Offset Voltage Distribution

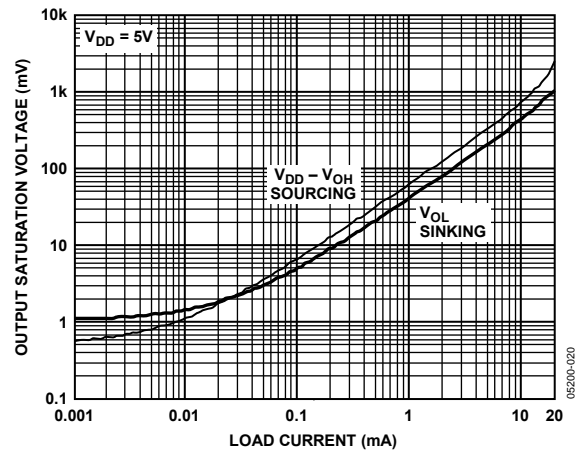


Figure 28. Output Swing vs. Load Current

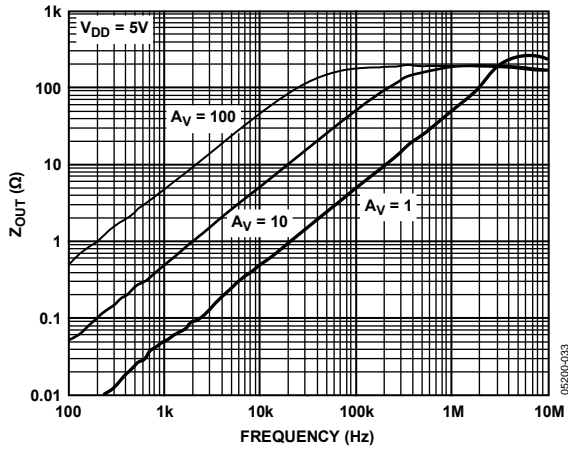


Figure 29. Closed-Loop Output Impedance vs. Frequency

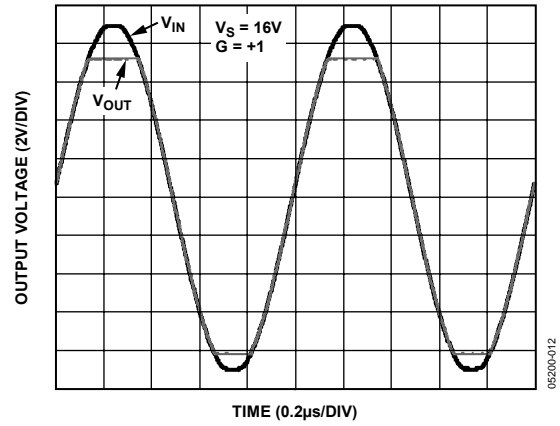


Figure 31. No Phase Reversal

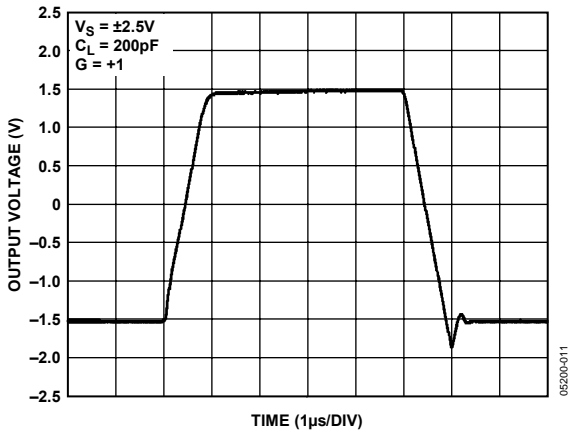
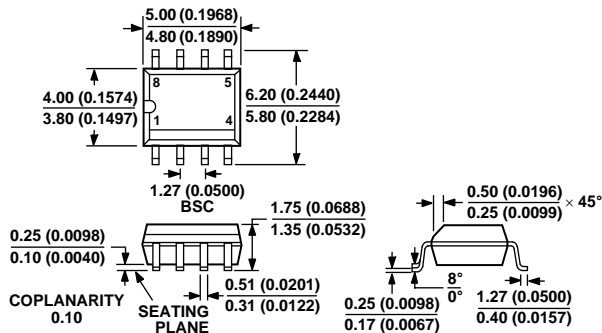


Figure 30. Large Signal Transient Response

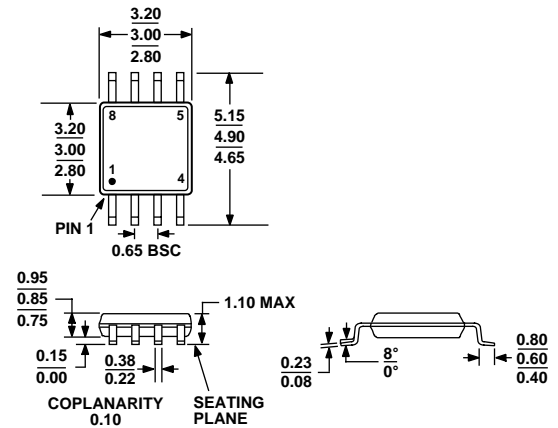
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 32. 8-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA
Figure 34. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

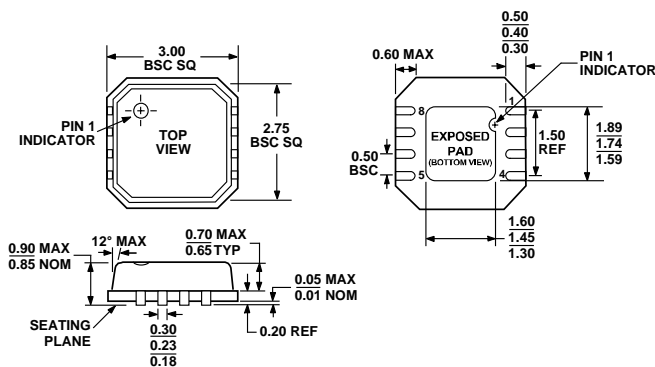


Figure 33. 8-Lead Lead Frame Chip Scale Package [LF CSP_VD]
3 mm x 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8661ARZ ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8661ARZ-REEL ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8661ARZ-REEL7 ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8661ACPZ-R2 ¹	-40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	A0M
AD8661ACPZ-REEL ¹	-40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	A0M
AD8661ACPZ-REEL7 ¹	-40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	A0M
AD8662ARZ ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8662ARZ-REEL ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8662ARZ-REEL7 ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8662ARMZ-R2 ¹	-40°C to +125°C	8-Lead MSOP	RM-8	A10
AD8662ARMZ-REEL ¹	-40°C to +125°C	8-Lead MSOP	RM-8	A10

¹ Z = Pb-free part.

AD8661/AD8662

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AD8661/AD8662

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